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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,552	03/30/2005	Tatsuya Kamei	XA-10260	9339

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
NGUYEN, THAN VINH	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,552	KAMEI ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

2. The IDS, filed 6/7/05, has been considered.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A Data Processor To Control Block Transfer of An Internal Memory.

Claim Rejections - 35 USC § 112

4. Claims 2,3 recites the limitation "the other of the transfer source" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to which address Applicant is referring to.

5. Claims 4,5,14,15 are also rejected for incorporating the above errors of the parent claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-10,12,14-17,20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagayasu (US 6,801,988).

As to claim 1,16,20:

8. Nagayasu teaches a data processor comprising: a CPU (CPU 1); a cache (cache 4); an internal memory accessible by said CPU (SDRAM 3); and a control circuit (memory controller 2) capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as one transfer object, wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request (transfer command 2/50-57; 4/19), the particular instruction has an addressing field , and when an address specified by the addressing field coincides with an address mapped to said internal memory, the address is set as one of transfer source and transfer destination addresses of the block transfer (destination address of data transfer; 2/20-33).

As to claim 2:

9. Nagayasu teaches wherein the other of the transfer source and transfer destination addresses of the block transfer is a physical address corresponding to a logical address held by the addressing field (physical address; 4/10-17).

As to claim 3:

10. Nagayasu teaches wherein the other of the transfer source and transfer destination addresses of the block transfer is a physical address held by a register (address register 13).

As to claim 4:

Nagayasu wherein said register is mapped to an address space of said CPU (4/10-12; 4/54).

As to claim 5,14,15:

11. Nagayasu teaches a bus interface controller connected to said control circuit, wherein said bus interface controller is capable of performing interface control of the other transfer object (address/data bus CADD/CDATA; Fig. 1).

As to claim 6:

12. Nagayasu teaches a cache memory, wherein said cache memory shares a first bus with said CPU, internal memory, and control circuit (cache 4; 4/25-35).

As to claim 7:

13. Nagayasu teaches wherein said internal memory is assigned a cache non-object address for said cache memory (cache address different from SDRAM address; 4/40-44).

As to claim 8,17:

14. Nagayasu teaches a second bus used exclusively for connecting said control circuit with said internal memory, wherein said second bus can be utilized for data block transfer in response to the particular access request (MDATA, MADD, MDS buses; 4/25-35).

As to claim 9:

15. Nagayasu teaches control circuit is capable of performing memory control in regard to a cache hit and cache miss with respect to said cache memory (4/36-44).

As to claim 10:

16. Nagayasu teaches the set of instructions for said CPU includes a first cache memory-operating instruction, and the first cache memory-operating instruction causes an operation of making said cache memory retain data at a cache object address specified by the addressing field (4/36-44).

As to claim 12:

17. Nagayasu teaches the particular instruction has an operation code identical with that of the first cache memory-operating instruction, and sets the cache non-object address of the addressing field as the destination address (write to cache; 4/40/44).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 11,13,18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayasu (US 6,801,988) in view of Spencer et al (US 6,772,295).

As to claim 11,18:

20. Nagayasu does not specifically teach determining if cache hit is dirty and to writeback the dirty data. It is well-known in the art to use cache coherency protocols (such as MESI) to

maintain data consistency in the cache. Spencer teaches checking if data in a cache is dirty and to writeback the dirty data to the main memory to maintain cache consistency. Thus, it would have been obvious to one of ordinary skills to incorporate Spencer's teachings of writing back dirty data to the main memory so that data coherency can be maintained.

As to claim 13,19:

21. Nagayasu the particular instruction has an operation code identical with that of the second cache memory-operating instruction, and sets the cache non-object address of the addressing field as the source address (set destination address of data transfer; 2/20-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Than Nguyen
Primary Examiner
Art Unit 2187